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Transmitted herewith for filing is the patent application of:

Inventors: **Roberto CAPPELLETTI**
Giuseppe CANTONE

For: **MULTICHANNEL TRANSCEIVER OF DIGITAL SIGNALS OVER POWER LINES**

Enclosed are:

[X] Patent Application: 22 pages, 6 claims.
[X] 7 Sheets of drawings.
[X] A Preliminary Amendment.
[X] Citation Under 37 CFR 1.97 and PTO-1449.

The Declaration and Filing Fee are **NOT ENCLOSED.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
CAPPELLETTI ET AL.

Serial No. **Not yet assigned**

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For: **MULTICHANNEL TRANSCEIVER OF DIGITAL SIGNALS OVER POWER LINES**

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
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Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 6.

Please add new Claims 7 to 42.

7. A data transceiver station comprising:

a modem to be connected to a transmission line for receiving digital data;

a microprocessor connected to said modem for receiving demodulated digital data therefrom according to a Packet Mode transmission or a Bit Mode transmission; and

an interface circuit connected between said microprocessor and said modem and switching between a Packet

Mode and a Bit Mode during transfer of the demodulated digital data to said microprocessor, the switching being based upon whether the received digital data is a Packet Mode transmission or a Bit Mode transmission.

8. A data transceiver station according to Claim 7 wherein the transmission line comprises an electrical power line that is part of an electrical power distribution network; and wherein said modem generates information on detection of a voltage level greater than a threshold in a frequency band selected for transmission over the electrical power line.

9. A data transceiver station according to Claim 8 further comprising a zero-crossing circuit for detecting a zero-crossing of the voltage level and for producing a logic signal in response thereto that is input to said modem.

10. A data transceiver station according to Claim 7 wherein said serial interface comprises a receiver section and a transmitter section connected thereto, said transmitter section comprising:

a logic processing circuit for organizing the demodulated digital data into a stream of data structured in packets, and

a multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the stream of data structured in packets, and an output for providing the demodulated digital data or the stream of data structured in packets based upon a selection signal.

11. A data transceiver station according to Claim 7 further comprising an oscillator connected to said modem for providing carrier frequencies thereto.

12. A data transceiver station according to Claim 10 further comprising a memory connected to said logic processing circuit.

13. A data transceiver station according to Claim 10 wherein said logic processing circuit has an input for receiving a first clock signal corresponding to the demodulated digital data; and wherein said logic processing circuit provides a third clock signal comprising a sequence of N pulses having a second clock signal that is a multiple of a frequency of the first clock signal.

14. A data transceiver station according to Claim 10 wherein said multiplexer has a third input for receiving the first clock signal and a fourth input for receiving a fourth clock signal equal to the third clock signal or to the first clock signal based upon whether the selection signal corresponds to the demodulated digital data or the stream of data structured in packets.

15. A data transceiver station according to Claim 10 further comprising a memory connected to said logic processing circuit, wherein said memory comprises:

a first register having a first input for receiving the demodulated digital data and a second input for receiving a first register clock signal, and an output for providing a first data signal; and

a second register having a first input for receiving the demodulated digital data and a second input for receiving a second register clock signal, and an output for providing a second data signal.

16. A data transceiver station according to Claim 15 wherein said logic processing circuit further comprises:

a first counter having an input for receiving the first clock signal and an output for providing a first end-computation signal when N pulses have been counted; and

a second counter having an input for receiving a second clock signal, and an output for providing a second end-computation signal that is enabled by the first end-computation signal and disabled when said second counter counts N pulses of the second clock signal.

17. A data transceiver station according to Claim 15 wherein said logic processing circuit further comprises:

a second multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the third clock signal, and an output for providing the first register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon a switching signal that toggles every N pulses of the first clock signal; and

a third multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the third clock signal, and an output for providing the second register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon the switching signal.

18. A data transceiver station according to Claim 17 wherein said logic processing circuit further comprises a logic AND gate having a first input for receiving the second clock signal and a second input for receiving the second end-computation signal, and an output for providing the third clock signal as periodic sequences of the N pulses when the second clock signal is output at each enablement of the first end-computation signal.

19. A data transceiver station according to Claim 18 wherein said logic processing circuit further comprises a fourth multiplexer having a first input for receiving the first data signal and a second input for receiving the second data signal, and an output for providing a third data signal corresponding to the first data signal or to the second data signal based upon the switching signal.

20. A data transceiver station according to Claim 7 wherein said modem comprises at least one control register for storing the received digital data and for controlling verification thereof.

21. A data transceiver station according to Claim 7 wherein the demodulated digital data is based upon frequency shift keying demodulation.

22. A monolithic integrated multichannel transceiver comprising:

a modem having an input to be connected to an electrical power line of an electrical distribution power network for receiving digital data and an output for providing

a demodulated bit stream in response to the received digital data, said modem for detecting a voltage level in a frequency band selected for transmission over the electrical power line and for providing a logic signal when the voltage level exceeds a threshold;

a serial interface connected to said modem for providing a selection signal based upon the received digital data, said serial interface comprising a receiver section and a transmitter section connected thereto, said transmitter section comprising

a logic processing circuit for organizing the demodulated bit stream into a stream of data structured in packets, and

a multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the stream of data structured in packets, and an output for providing the demodulated bit stream or the stream of data structured in packets based upon the selection signal; and

a zero-crossing circuit connected to an external coupling circuit connected to the electrical power line for detecting a zero-crossing of the voltage level thereon and for providing an output logic signal to said modem in response to the zero-crossing of the voltage level.

23. A monolithic integrated multichannel transceiver according to Claim 22 wherein the demodulated bit stream corresponds to a Bit Mode transmission and the stream of data structured in packets corresponds to a Packet Mode transmission.

24. A monolithic integrated multichannel transceiver according to Claim 22 wherein said modem comprises at least one control register for storing the received digital data and for controlling verification thereof.

25. A monolithic integrated multichannel transceiver according to Claim 22 further comprising an oscillator connected to said modem for providing carrier frequencies thereto.

26. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a memory connected to said logic processing circuit.

27. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a power interface circuit connected to said modem and for driving the external coupling circuit.

28. A monolithic integrated multichannel transceiver according to Claim 22 wherein said logic processing circuit has an input for receiving a first clock signal corresponding to the demodulated bit stream; and wherein said logic processing circuit provides a third clock signal comprising a sequence of N pulses having a second clock signal that is a multiple of a frequency of the first clock signal.

29. A monolithic integrated multichannel transceiver according to Claim 22 wherein said multiplexer has a third input for receiving the first clock signal and a

fourth input for receiving a fourth clock signal equal to the third clock signal or to the first clock signal based upon whether the selection signal corresponds to the demodulated bit stream or the stream of data structured in packets.

30. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a memory connected to said logic processing circuit, wherein said memory comprises:

a first register having a first input for receiving the demodulated bit stream and a second input for receiving a first register clock signal, and an output for providing a first data signal; and

a second register having a first input for receiving the demodulated bit stream and a second input for receiving a second register clock signal, and an output for providing a second data signal.

31. A monolithic integrated multichannel transceiver according to Claim 30 wherein said logic processing circuit further comprises:

a first counter having an input for receiving the first clock signal and an output for providing a first end-computation signal when N pulses have been counted; and

a second counter having an input for receiving a second clock signal, and an output for providing a second end-computation signal that is enabled by the first end-computation signal and disabled when said second counter counts N pulses of the second clock signal.

32. A monolithic integrated multichannel

transceiver according to Claim 30 wherein said logic processing circuit further comprises:

a second multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the third clock signal, and an output for providing the first register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon a switching signal that toggles every N pulses of the first clock signal; and

a third multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the third clock signal, and an output for providing the second register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon the switching signal.

33. A monolithic integrated multichannel transceiver according to Claim 31 wherein said logic processing circuit further comprises a logic AND gate having a first input for receiving the second clock signal and a second input for receiving the second end-computation signal, and an output for providing the third clock signal as periodic sequences of the N pulses when the second clock signal is output at each enablement of the first end-computation signal.

34. A monolithic integrated multichannel transceiver according to Claim 32 wherein said logic processing circuit further comprises a fourth multiplexer having a first input for receiving the first data signal and a second input for receiving the second data signal, and an output for providing a third data signal corresponding to the

first data signal or to the second data signal based upon the switching signal.

35. A method of using a data transceiver station for exchanging digital data over an electrical power line, the data transceiver station comprising a modem connected to the electrical power line, an interface circuit connected to the modem, and a microprocessor connected to the interface circuit, the method comprising:

demodulating the digital data using the modem;

switching the interface circuit between a Packet Mode and a Bit Mode based upon whether the received digital data is a Packet Mode transmission or a Bit Mode transmission; and

transferring the demodulated digital data from the modem to the microprocessor.

36. A method according to Claim 35 wherein demodulating the digital data comprises providing a demodulated bit stream to the serial interface.

37. A method according to Claim 36 further comprising organizing the demodulated bit stream into a stream of data structured in packets.

38. A method according to Claim 37 further comprising providing to a first input of a multiplexer the demodulated bit stream and to a second input of the multiplexer the stream of data structured in packets, and providing at an output of the multiplexer the demodulated bit

stream or the stream of data structured in packets based upon a selection signal.

39. A method according to Claim 38 further comprising generating the selection signal based upon the received digital data.

40. A method according to Claim 35 further comprising:

detecting a zero-crossing of a voltage level on the electrical power line; and

providing an output logic signal to the modem in response to the zero-crossing of the voltage level.

41. A method according to Claim 35 further comprising:

detecting a voltage level in a frequency band selected for transmission over the electrical power line; and

producing a logic signal when the voltage level exceeds a threshold.

42. A method according to Claim 35 wherein the modem comprises at least one control register for storing the digital data and for controlling verification thereof.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course.

In re Patent Application of:
CAPPELLETTI ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**
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Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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MULTICHANNEL TRANSCEIVER OF DIGITAL SIGNALS OVER POWER LINES

Field of the Invention

The present invention relates to data transmission systems, and, more particularly, to a digital signal transceiver for home applications, specially, though not exclusively, coupled to an electrical power distribution line.

Background of the Invention

Electric power distribution networks are widespread and are capillary like. These networks primarily transport and distribute electric energy, but the possibility of exploiting it also as a medium for data transmission is well known. Electrical mains can be advantageously used to establish communication with far away locations exploiting the fact that even remote rural users are reached by an electrical power line. It is also possible to avoid the cost of a dedicated line (e.g., a telephone line) for telecommunications.

Data transmission on electrical mains is possible since AC power is distributed with a well determined frequency. Signal modulation techniques permit the transmission of information on or about a certain carrier frequency that may advantageously be in a frequency band not occupied by other signals. It is

possible to transmit on the same line several signals, each occupying a different frequency band. The receiver selects the desired signal by tuning to the relative carrier frequency.

Data transmission on power lines may be a particularly efficient technique for controlling machines installed in a remote location, without being forced to install a dedicated telecommunication line. Because of the advantages provided by such a data transmission technique, transceivers for coupling to power lines have an increasing importance.

A telecommunication station coupled to power lines generally includes a microprocessor interfaced with a transceiver coupled to the power line. Power line transceivers are well known and commercially available. Examples of effective transceivers are described in U.S. Patent No. 4,714,912 and U.S. Patent No. 5,842,032.

Generally, known transceivers do not directly interface with a microprocessor. Moreover, these transceivers require dedicated interface devices for coupling with the electrical mains to meet the requirements of the communication standards on the network, establishing access criterions, avoiding frequency bands reserved to electricity producers and frequency bands reserved for home applications. It would be desirable to have a fully integrated transceiver allowing the realization of a telecommunication station with the above mentioned characteristics, capable of supporting the remote managing of electrical loads connected to the electrical mains.

Often the conditions for using such a telecommunication system on electrical power lines are those of communicating with people at their homes, such

as in applications generally referred as home applications. In these application areas, the cost of apparatuses has a great importance.

Usually a digital data transceiving station specifically uses a multichannel transceiver coupled through an appropriate interface to an electrical power distribution network. Also, the digital data transceiving station may generally comprise a modem interfaced with a microprocessor by way of a specific communication circuit between the modem and the microprocessor, commonly called a serial interface.

In known systems, the possible choices are either to establish a Bit Mode or a Packet Mode communication between the modem and the microprocessor through the serial interface. Binary serial transmission between the modem and the microprocessor can be made in two different ways. The first is the data transceiving station, where each time the modem has a demodulated bit, it transmits it to the microprocessor. The second is the Packet Mode. In this mode the modem stores a pre-established number of bits forming a packet of bits that eventually is transmitted to the microprocessor.

Bit Mode communication between the modem and the microprocessor does not introduce any data format because bits are transmitted immediately after the modem has decoded them. It is easy to understand that the Bit Mode has the advantage of being usable irrespective of any particular data format, but its drawback is that the rate of communication between the modem and the microprocessor is limited to that of the communication channel.

In contrast, in Packet Mode communication the rate of communication between the modem and the microprocessor can be greater than that over the

channel. However, it is not independent of the particular data format. Bit Mode communication ensures compatibility of the system irrespective of the data format used, but this approach imposes the use of a microprocessor having adequate computing capacities to interpret the bit stream received by the serial interface for its information content.

The technical alternative of establishing a Packet Mode communication between the modem and the microprocessor is advantageous because it ensures a faster communication and allows the use of a relatively low cost microprocessor for the same global performances of the station. However, it is usable only by operating with a certain predefined data format.

For example, if the protocol format has data in frames being transmitted with a preamble followed by a header and by a data field alternated with synchronization signals, formatting the preamble into packets would destroy its information content. If data were formatted in M bit words and the Packet Mode transmission forms packets of N bits, the microprocessor would be forced to process the received data to extract the original M bit words. This would waste the benefits of the greater communication speed that may be achieved with a Packet Mode transmission.

Therefore, there is a clear need and/or utility of having a digital data transceiver wherein communication between the modem and the microprocessor through the serial interface may switch back and forth between a Bit Mode and a Packet Mode during the time slot in which a single data frame is transmitted. This switching is done without any loss of data.

Summary of the Invention

An object of the present invention is to provide a digital data transceiving station joining together in an optimal manner the advantages of a Packet Mode transmission with the advantages of a Bit Mode transmission, thus providing enhanced speed performances even using a relatively low cost microprocessor.

The transceiving station of the invention is characterized in that during the transmission of each single data frame between the modem and the microprocessor, the serial interface switchs from a Packet Mode to a Bit Mode communication without losing data.

According to a preferred embodiment of the invention, the data transceiver of the invention is directly connectable to a coupling circuit to a line of a power distribution network via an integrated interface circuit. The modem produces an information of detection in a selected transmission band of a signal energy level greater than a pre-established threshold level. Preferably, the integrated data transceiver of the invention also comprises a circuit that detects the zero crossing of the power network voltage. This produces a logic signal that is input to the modem.

According to another aspect of the invention, the station is based on the use of a monolithically integrated multichannel transceiver of digital data to be connected to a line of a power distribution network. The transceiver comprises a modem having a register for data storage, and a circuit for controlling their integrity and for signaling the eventual corruption of at least one bit. A serial interface communicates with an external microprocessor. The transceiver further

includes an oscillator generating carrier frequencies that are fed to the modem, and a power line interface circuit coupled to the modem for driving an external circuit coupling with the power line. A circuit detects the zero-crossing of the network voltage and produces a logic signal that is fed to an input of the modem.

According to the present invention, the data transmission section of the serial interface of the transceiver includes a buffer and a logic circuit that processes the demodulated bit stream coming from the modem. The logic circuit is enabled by an enabling signal and functions with a clock having a frequency multiple of the demodulated bit stream frequency. The enabling signal and the multiple clock signal are both generated by a control logic circuit of the serial interface as a function of a command issued by an external microprocessor.

A multiplexer receives on a first input the nonformatted bit stream output by the modem and on a second input a packet reorganized data flow produced by the processing circuit. The same enabling signal of the processing circuit operates also the selection by the multiplexer, outputting towards the external microprocessor a bit stream (Bit Mode) as decoded by the modem or a flow of data organized in packets (Packet Mode) from the processing circuit.

Brief Description of the Drawings

The different aspects and advantages of the invention will be evidenced in the following description of embodiments of the invention and by referring to the attached drawings, wherein:

Figure 1 is a general block diagram of the

integrated transceiver according to the present invention;

Figure 2 is a more detailed block diagram of certain blocks of the general diagram illustrated in Figure 1, according to an embodiment of the present invention;

Figure 3 is a block diagram of the serial interface of the integrated transceiver according to the present invention;

Figure 4a is a circuit diagram of the transmitting section of the serial interface of the transceiver according to the present invention;

Figure 4b is a timing of important signals of the transmitting section of the serial interface illustrated in Figure 4a;

Figure 5a illustrates a transceiving station coupled to a power distribution line according to the present invention;

Figure 5b illustrates a circuit according to the present invention for coupling the transceiver to a power network line.

Detailed Description of the Preferred Embodiments

The integrated transceiver of the invention is depicted schematically in Figure 1, and is formed by a digital modem MODEM which may be a frequency shift keying (FSK) modem, for example. A serial interface circuit SERIAL_INTERFACE allows the modem to communicate external the integrated transceiver. The integrated transceiver further includes an oscillator OSCILLATOR providing carrier frequencies to the modem, a power interface PLI for driving an external coupling circuit to a line of the electrical power distribution network, and a zero-cross detector ZC of the network voltage.

Optionally, a monolithically integrated voltage regulator VREG is also present for powering other ICs that may be present in the transceiving station.

During a receiving phase, the signal derived from the power network line is received on the pin RAI, demodulated and made available on the pin DATA_OUT. Optionally, the transceiver may produce on the pin CLR/T a clock signal for bit synchronization. The integrated transceiver provides on the pin BU information about the detection of an energy level greater than a fixed threshold, e.g., 80 dBμV, in a selected frequency band. Such information allows the use of the communication channel on an electrical power line in the frequency band reserved to home applications.

According to the CENELEC EN 50065-1 rules defining the European criteria for access to such a telecommunication medium, it is prohibited to transmit in the frequency band reserved to home applications if on the channel there is a signal stronger than 80 dBμV. By having the modem implementing this energy detection function in a selected band, realization of dedicated external circuitry for filtering and amplitude monitoring is avoided.

Another peculiarity of the integrated circuit of the invention is the fact that it integrates a circuit ZC that detects the zero-crossing of the network voltage by comparing a replica signal of the network voltage fed to the pin ZCIN. The zero-crossing information is produced on the pin ZCOUT, and in addition to making it available to the external world (microprocessor) it is input to the modem for synchronizing the transmission with the zero-crossing of the network voltage.

In this way, appliances connected to the electrical power network, besides receiving command data sent by the transceiver, receive also the information of the instant in which the network voltage is zero. Such information is useful to drive certain electric loads. Knowing the instant in which the network voltage is zero may be usefully exploited for determining the turn-on and turn-off instants of loads. This avoids voltage peaks on power switches. When there is not a need to synchronize the transmission with the zero-crossing of the network voltage, the transceiver may be programmed to ignore the relative signal on the ZCOUT mode.

A preferred embodiment of the integrated transceiver of the invention is depicted in Figure 2, wherein different blocks forming the modem are highlighted. In the illustrated example, the modem is an FSK type. The signal present on the pin RAI is demodulated by a receiver, such as a superheterodyne receiver, for example. The demodulated signal is fed to a CLOCK_RECOVERY block.

The signal present on the pin RAI is filtered and made available after the band-pass filter on the pin RXFO. This provides a measure of the power of the signal in the selected band. The pin CD/PD of the transceiver of the invention has two functions. Through this pin the presence of a carrier in the selected channel (carrier detection) can be signaled independently of the amplitude of the carrier. This is for communicating the possibility that a message could be arriving. The detection threshold is determined by the modem sensitivity at the input pin RAI. The other function is to communicate that a bit stream is being received with the selected bit-rate (preamble detection).

Upon recovering the clock signal, the block FSK_DEMODULATOR provides the demodulated signal to the SERIAL_INTERFACE block which outputs it on the pin DATA_OUT. The SERIAL INTERFACE block conveys data from the FSK_DEMODULATOR to the outside world and from the outside world to the FSK_MODULATOR. This is done under the control of a signal TX/RX specifying which one of the two operations must be carried out.

Moreover, the transceiver is provided with a control register CONTROL_REGISTER where the parameters necessary to the transceiver are stored. These parameters define the modem configuration. Because of the high electromagnetic noise that is normally present on the power line, the content of the CONTROL_REGISTER is continuously monitored to ensure a reliable security margin on the integrity of the data stored in it. In case of corruption of the stored data, an alarm signal is produced on the pin REG_OK.

Moreover, the CONTROL_REGISTER is provided with a pin TIMEOUT to support the use of protocols that contemplate the interruption of the transmission at pre-established time intervals, as measured by the block TIMER. The CONTROL_REGISTER can be externally programmed by way of the control signal REG_DATA. Such a signal communicates to the SERIAL_INTERFACE whether the signal DATA_IN, coming from outside, is data to store in the CONTROL_REGISTER or is data to be fed to the FSK_MODULATOR. By programming the CONTROL_REGISTER it is possible to make the information on preamble detection available on the pin CD/PD.

The signal produced by the FSK_MODULATOR is filtered by a programmable band pass filter FILTER which reduces all undesired harmonic components to reduce the electromagnetic noise. The filtered signal is input to the power interface PLI by way of an

amplitude control stage ALC. Regulation of the voltage level and of the current level of the transmitted signal is performed by the relative blocks of current mode control CURRENT_CONTROL and of voltage mode control VOLTAGE_CONTROL. These signals are representative of the current CL and of the voltage VSENSE.

The transmission carrier frequencies are derived from the oscillation of an external quartz coupled to the pins XTAL1 and XTAL2. The oscillation is kept resonant by an excitation circuit integrated in the device. Preferably, the excitation circuit includes a MOS stage operating below its threshold level to limit absorption. From the oscillator is derived a clock signal that is made available on the pin MCLK to drive an external microprocessor for optionally avoiding use of other resonators.

Preferably, the transceiver has a pin WD dedicated to the supervision of the transmission. To preserve the communication channel, the transceiver monitors the signal present on the pin WD. If during a pre-established time interval, as measured by the block TIMER, no transition has been observed, the control register interprets this fact as a failure and communicates to the external world an alarm by way of the signal RSTO.

The signal RSTO can be conveniently used even to signal the presence of a voltage level, as produced by the regulator VREG, insufficient to make the transceiver station operate correctly. To this effect, the voltage regulator VREG is provided with a pin PG on which the information of the presence of an output voltage of the regulator VREG greater than a minimum pre-established value is provided, such as 4 to 5 V, for example.

In Figure 2 the supply pins for the digital and analog sections are indicated by DVdd, DVss, Avdd, and AVss, and the supply pin of the power interface is PAVcc. The pin TEST is used for functionality testing of the integrated device.

A diagram of the SERIAL_INTERFACE block is depicted in Figure 3. It comprises a receiving section RX_SECTION, a transmitting section TX_SECTION, and a SERIAL_INTERFACE_CONTROL_UNIT. The line SIGNAL_GROUND provides the reference voltage for data reading. The receiving section RX_SECTION receives a data signal DATA_IN and produces an output signal DATA_SEND that is fed either to the FSK_MODULATOR block or to the CONTROL_REGISTER, depending on the control signal REG_DATA.

The TX_SECTION comprises a logic processing circuit BUFFER_CONTROL_UNIT using a working memory, BUFFER, and an output MULTIPLEXER. The BUFFER_CONTROL_UNIT receives the bit stream RECOVERED_DATA output by the demodulator at a certain clock frequency RECOVERED_CLOCK, and uses a clock signal BURST_CLOCK having a frequency that is generally a multiple of the frequency of the clock of the received bit stream. This is done to perform data organization in packets according to a certain format.

When enabled by the enabling signal BURST_ENABLE, the logic processing circuit BUFFER_CONTROL_UNIT reads the data stored in the working memory BUFFER at the scanning frequency of the BURST_CLOCK and produces on an input of the MULTIPLEXER a data stream BC organized according to a Packet Mode format.

The input bit stream RECOVERED_DATA, besides being fed to the logic processing circuit, is also fed to a second input of the MULTIPLEXER. The SERIAL_INTERFACE_CONTROL_UNIT, besides activating

alternately the receiving section RX_SECTION and the transmitting section TX_SECTION, depends on an external command TX/RX. The signal BURST_ENABLE and the clock signal BURST_CLOCK are produced with a frequency multiple of the clock frequency of the bit stream, and is used by the BUFFER_CONTROL_UNIT and by the MULTIPLEXER to operate the mode selection.

Optionally, even a clock signal (CLR/T) relative to the selection of a data flow in the Bit Mode or in the Packet Mode can be output. In this case, the logic processing circuit BUFFER_CONTROL_UNIT feeds to other inputs of the MULTIPLEXER a third clock signal A formed by sequences of a pre-established number of pulses of the BURST_CLOCK. These pulses are periodically generated at pre-established intervals and are applied to the clock of the input bit stream RECOVERED_CLOCK.

The BURST_ENABLE signal enables or disables the logic processing circuit BUFFER_CONTROL_UNIT and selects using the MULTIPLEXER the output data stream DATA_OUT. This corresponds to the input bit stream (Bit Mode) RECOVERED_DATA and optionally also the relative clock RECOVERED_CLOCK on the CLR/T output, or to the BC stream of data organized in packets (Packet Mode) by the BUFFER_CONTROL_UNIT and optionally also the relative clock signal A on the CLR/T output.

An effective embodiment of the transmitting section TX_SECTION of the serial interface is depicted in Figure 4a. The circuit is composed of a pair of shift registers SHIFT_REGISTER_1 and SHIFT_REGISTER_2, having the capacity equal to a bit length N of a packet. The two registers are paralleled, fed with the RECOVERED_DATA bit stream and their outputs are coupled to respective inputs of the multiplexer MUX3. The two registers store and unload the bits forming a packet.

Data storage is performed at a frequency equal to the bit stream frequency RECOVERED_CLOCK, while the data unloading is performed at the multiplied frequency of the BURST_CLOCK. A switching signal T, produced by the logic block TOGGLE, prevents the two registers SHIFT_REGISTER_1 and SHIFT_REGISTER_2 from performing the same operation at the same time. This insures that the multiplexer MUX3 coupled to the outputs of the registers coordinately selects the output of the register that is unloading the stored data. The signal T switches every N pulses of the RECOVERED_CLOCK, making the input multiplexers MUX1 and MUX2 feed the respective shift register. One is in synchronization with the RECOVERED_CLOCK and the other with a third clock signal A.

The modulus N first counter COUNTER_1 enabled by the BURST_ENABLE outputs a first end-computation signal C1 every N pulses of the RECOVERED_CLOCK. The first end-computation signal C1 makes the signal T switch, and enables the modulus N counter COUNTER_2 that produces a second end-computation signal C2 activated at the instant the counter is enabled for as long as N pulses of the BURST_CLOCK have been counted. Upon counting N pulses, COUNTER_2 disables the signal C2.

The third clock signal A is produced by performing a logic AND of the second end-computation signal C2 and of the BURST_CLOCK. Therefore, the clock signal A corresponds to the period of sequences of N pulses of the BURST_CLOCK repeating at each activation of the first end-computation signal C1.

Therefore, the multiplexers MUX1 and MUX2 are fed with a signal having N pulses of the BURST_CLOCK at the instant in which one of the two registers is full. Using the switching signal T, the N pulses are input to

the register that has just reached the full state, thus unloading the packet formed by the N bits stored in it.

To output also the clock signal CLR/T wherein the bits are output as DATA_OUT according to the selection operated between the Bit Mode and Packet Mode, it can be produced by a multiplexer MUX4 for outputting either the RECOVERED_CLOCK or the third clock signal A. This depends on whether the signal BURST_ENABLE establishes a Bit Mode or a Packet Mode transmission. An output multiplexer MUX5 outputs the bit stream DATA_OUT in Packet Mode or in Bit Mode according to the selection operated by the signal BURST_ENABLE.

The described architecture is just one among many according to the diagram of Figure 3. Other circuit approaches are possible. For example, a RAM memory or a circular register may be used instead of the pair of shift registers and by adapting the BUFFER_CONTROL_UNIT to produce the appropriate signals to manage the particular type of storages used.

The above described SERIAL_INTERFACE allows switching between Bit Mode and Packet Mode data transmission to the microprocessor by just varying the BURST_ENABLE signal during transmission of a data frame. This ability allows the transmission of the message to be sent exploiting both the versatility of a Bit Mode transmission and the superior speed of a Packet Mode transmission. A portion of the data frame may be transmitted in Bit Mode and the remaining portion in Packet Mode, and the two modes of transmission may alternate in whichever order without causing any bit loss while switching from one transmission mode to the other.

A timing diagram of the most important signals of the serial interface is depicted in Figure

4b. Generally, a data frame FRAME of the stream DATA_OUT can be split into a PREAMBLE, a HEADER and in a payload portion containing the data bits DATA interleaved by synchronization signals CRC.

The signal TX/RX switches for enabling the TX_SECTION of the SERIAL_INTERFACE. Given that it is not possible to transmit the bits belonging to the PREAMBLE and/or to the HEADER in Packet Mode because the information carried is in their bit-rate, the BURST_ENABLE signal switches to transmit the PREAMBLE and the HEADER in Bit Mode and the data bits DATA in Packet Mode.

Switching from a transmission mode to the other is not the only possible switching scheme. It is possible to command any number of switchings from Packet Mode to Bit Mode and viceversa during the transmission of a single data frame FRAME. During transmission in Packet Mode, the clock signal CLR/T is idle in certain time intervals, allowing the reading of the signal DATA_OUT only when the above mentioned sequences of N pulses of the BURST_CLOCK are present. This is highlighted in the enlarged detail of Figure 4b, wherein the DATA_OUT signal is read only when the CLR/T clock is not idle, and as depicted by way of an example in correspondence of its rising edge.

A sample scheme of a circuit of a transceiving station according to the present invention is depicted in Figure 5a. Substantially, the transceiving station is formed with the transceiver of Figure 2. Fundamentally, the receiving station comprises a digital modem coupled to a data transmission line, which in the example shown is a line of a power distribution network.

A microprocessor μP receives the data demodulated by the modem in Packet Mode or in Bit Mode

through the interface circuit SERIAL_INTERFACE that couples the modem to the microprocessor µP. The SERIAL_INTERFACE changes the transmission mode to the microprocessor of the demodulated data from a Packet Mode to a Bit Mode during the transmission of each single data frame, without any bit loss during the switching from one mode to the other.

A suitable circuit to couple the transceiver of the invention to the electrical power line is depicted in Figure 5b. The station may me made able to control electric loads connected to the power line by using the frequency bands that are reserved for this function. The station monitors the presence in the selected band of an energy level greater than a certain pre-established maximum threshold and accesses the transmission channel only if such a pre-established threshold may be equal to 80 dBµV. This meets the requirements of CENELEC EN 50065-1 rules that define the European standard in accessing electrical power lines for communications relative to home applications.

To improve the control of electric loads by avoiding undesired overvoltages on switches, the integrated transceiver of the invention includes a circuit ZC for detecting the zero-crossing of the network voltage.

THAT WHICH IS CLAIMED IS:

1. A data transceiving station of digital data frames comprising a digital modem (MODEM) coupled to a transmission line, a microprocessor (μP) receiving demodulated data from said modem according to a Packet Mode or a Bit Mode transmission, an interface circuit (SERIAL_INTERFACE) between said microprocessor (μP) and said digital modem (MODEM) characterized in that

said interface circuit (SERIAL_INTERFACE) switches from a Packet Mode to a Bit Mode transmission and/or viceversa during transfer of a data frame to said microprocessor.

2. The data transceiving station of claim 1, wherein said transmission line is a line of an electric power distribution network and said modem (MODEM) generates an information on the detection of an energy level greater than a pre-established threshold in a frequency band selected for transmission over said line.

3. The data transceiving station of claim 2, characterized in that it comprises a circuit (ZC) detecting the zero-crosses of the network voltage and producing a logic signal (ZCOUT) that is also input to said modem (MODEM).

4. A monolithically integrated multichannel transceiver of digital frames over a line of an electric distribution power network, comprising a modem (MODEM) having a register for data storage (CONTROL_REGISTER) and means for controlling their integrity and signalling any eventual corruption of at least one bit, a serial interface (SERIAL_INTERFACE),

including a receiving section (RX_SECTION) and a transmitting section (TX_SECTION), coupling said modem to the external world, an oscillator (OSCILLATOR) generating carrier frequencies fed to said modem, a power interface circuit (PLI), coupled to said modem and driving an external coupling circuit to said line, characterized in that it comprises

a circuit (ZC) detecting the zero-crosses of the network voltage and producing an output logic signal (ZCOUT) coupled to an input of said modem (MODEM) and to a pin of the transceiver;

said modem detecting the energy level in a certain frequency band selected for transmission over said line, producing a logic signal on a dedicated pin (BU) when said energy level surpasses a pre-established threshold;

said transmitting section (TX_SECTION) of the serial interface (SERIAL_INTERFACE) comprises a logic processing circuit (BUFFER_CONTROL_UNIT) and a work memory (BUFFER) for organizing a demodulated bit stream (RECOVERED_DATA)coming from the modem in a stream (BC) of data structured in packets, a multiplexer (MULTIPLEXER) receiving on a first input said demodulated bit stream (RECOVERED_DATA) and said stream of structured data (BC) and operating a selection between said two streams outputting (DATA_OUT) either a not structured Bit Mode bit stream or a Packet Mode data stream organized in packets, in function of a selection signal (BURST_ENABLE) and a control unit (SERIAL_INTERFACE_CONTROL_UNIT) producing said selection signal (BURST_ENABLE) and a clock signal (RECOVERED_CLOCK) of said input bit stream (RECOVERED_DATA).

5. The transceiver of claim 4 wherein said logic circuit processing (BUFFER_CONTROL_UNIT) produces a third clock signal (A)

constituted by sequences of N pulses of a second clock signal (BURST_CLOCK) having frequency multiple of the frequency of said clock signal (RECOVERED_CLOCK) of the input bit stream at pre-established intervals;

said multiplexer (MULTIPLEXER) receives said clock signal (RECOVERED_CLOCK) of the input bit stream (RECOVERED_DATA) and said third clock signal (A), outputting a fourth clock signal (CLR/T) equal to said third clock signal (A) or to said first clock signal (RECOVERED_CLOCK) depending on whether said selection signal (BURST_ENABLE) selects said not structured bit stream (RECOVERED_DATA) or said data flow structured in packets (BC).

6. The transceiver of claim 4 wherein said work memory (BUFFER) comprises a first register (SHIFT_REGISTER_1) and second register (SHIFT_REGISTER_2) fed with said demodulated datastream (RECOVERED_DATA), and clocked with respective clock signals (Z1, Z2), and outputting a first data signal (S1) and a second data signal (S2), respectively;

said logic processing circuit (BUFFER_CONTROL_UNIT) comprises

a first modulus N counter (COUNTER_1) fed with said first clock signal (RECOVERED_CLOCK) producing a first end-computation signal (C1) when N pulses have been counted,

a second modulus N counter (COUNTER_2) fed with said second clock signal (BURST_CLOCK) and enabled by said first end-computation signal (C1), producing a second end-computation signal (C2) that is enabled by said first end-computation signal (C1) and disabled when said second counter (COUNTER_2) counts N pulses of said second clock signal (BURST_CLOCK),

a second multiplexer (MUX_1) and third multiplexer (MUX_2) fed with said demodulated bit stream (RECOVERED_DATA) and with said third clock signal (A) producing respectively said clock signals (Z1, Z2) corresponding alternately to said third clock signal (A) and to said first clock signal (RECOVERED_CLOCK), depending on a switching signal (T),that toggles every N pulses of said first clock signal;

a logic AND gate, combining said second clock signal (BURST_CLOCK) and said second end-computation signal (C2), producing said third clock signal (A) as periodic sequences of N pulses of said second clock signal (BURST_CLOCK) output at each enablement of said first end-computation signal (C1),

a fourth multiplexer (MUX_3) fed with said first data signal (S1) and with said second data signal (S2) and outputting a third data signal (BC) corresponding to said first data signal (S1) or to said second data signal (S2) depending on said switching signal (T).

MULTICHANNEL TRANSCEIVER OF DIGITAL SIGNALS OVER POWER LINES

Abstract of the Disclosure

A data transceiving station of digital data frames includes a digital modem coupled to a transmission line, and a microprocessor receiving demodulated data from the modem according to a Packet Mode or a Bit Mode transmission through an interface circuit. The interface circuit switches between the Packet Mode and the Bit Mode transmission during transfer of a data frame to the microprocessor. The data transceiving station combines the superior speed of a Packet Mode transfer with the unlimited compatibility of a Bit Mode transfer.

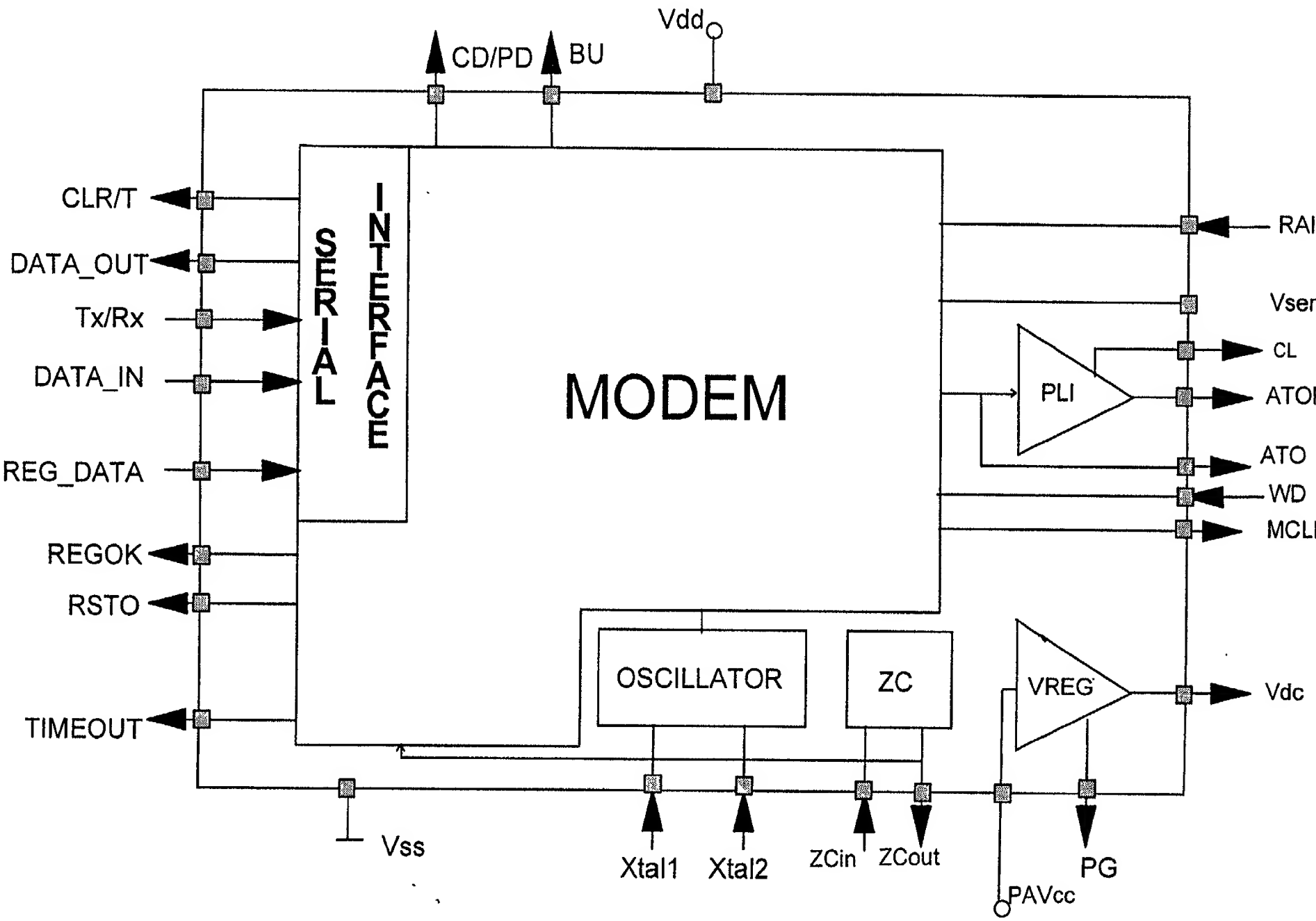

Vdd
CD/PD
BU
CLR/T
DATA_OUT
Tx/Rx
DATA_IN
REG_DATA
REGOK
RSTO
TIMEOUT
SERIAL INTERFACE
MODEM
RAI
Vsense
CL
ATOP
ATO
WD
MCLK
PLI
OSCILLATOR
ZC
VREG
Vdc
Vss
Xtal1
Xtal2
ZCin
ZCout
PG
PAVcc

fig. 1

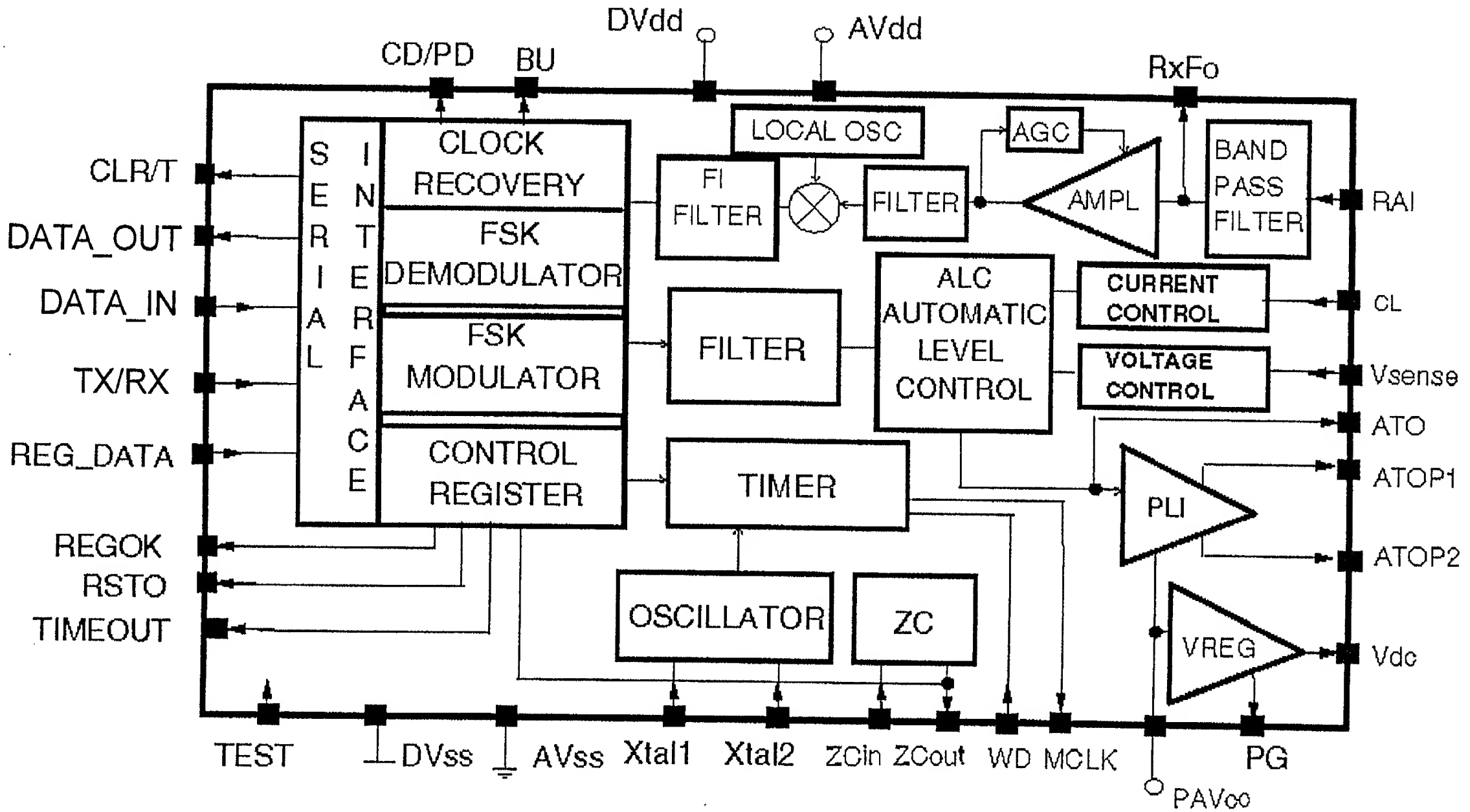

DVdd
AVdd
CD/PD
BU
RxFo
CLR/T
DATA_OUT
DATA_IN
TX/RX
REG_DATA
REGOK
RSTO
TIMEOUT
SERIAL INTERFACE
CLOCK RECOVERY
FSK DEMODULATOR
FSK MODULATOR
CONTROL REGISTER
LOCAL OSC
FI FILTER
FILTER
AGC
AMPL
BAND PASS FILTER
RAI
FILTER
ALC AUTOMATIC LEVEL CONTROL
CURRENT CONTROL
VOLTAGE CONTROL
CL
Vsense
ATO
ATOP1
ATOP2
PLI
TIMER
OSCILLATOR
ZC
VREG
Vdc
TEST
DVss
AVss
Xtal1
Xtal2
ZCin
ZCout
WD
MCLK
PG
PAVcc

fig. 2

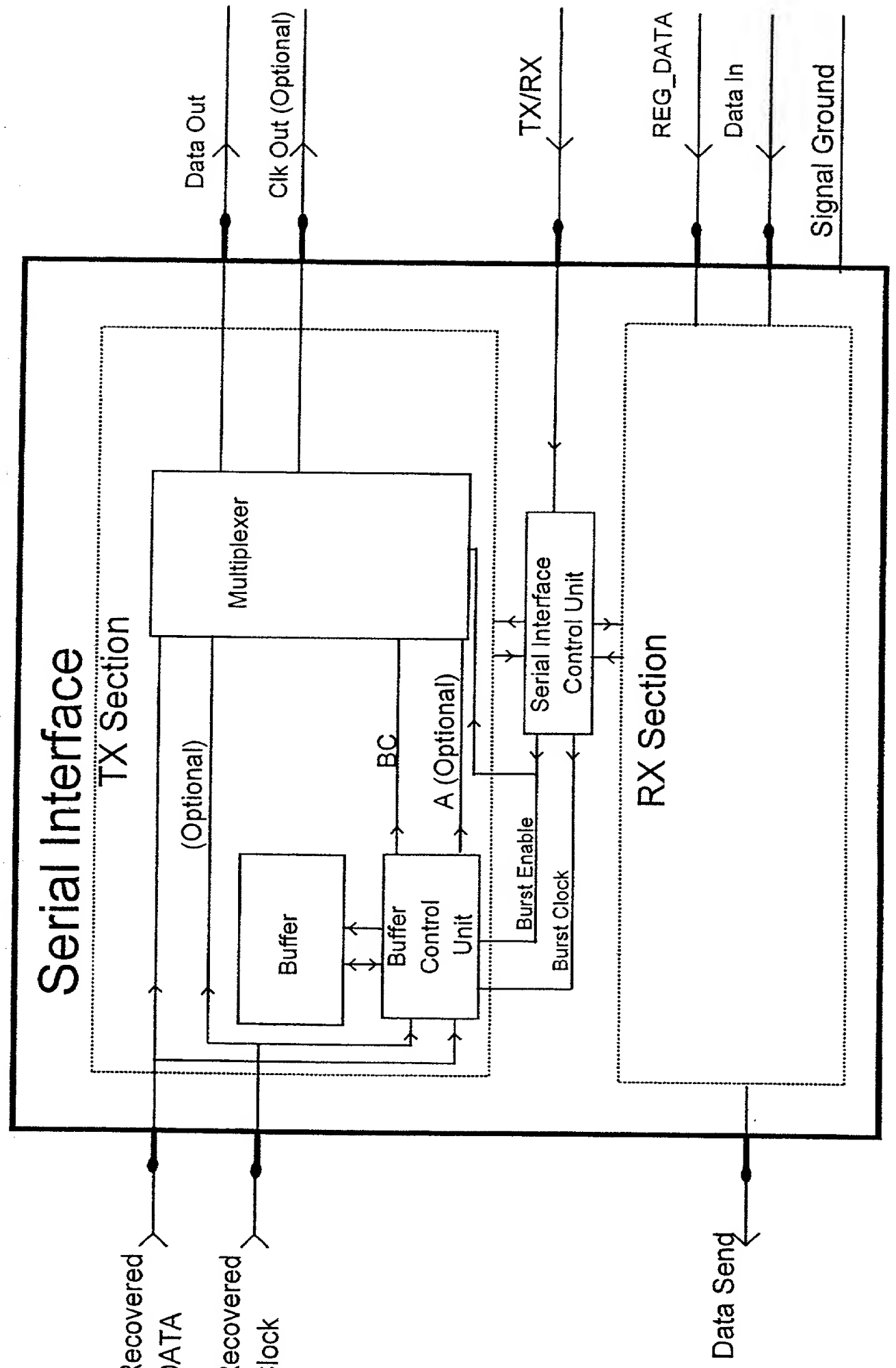

Serial Interface
TX Section
RX Section
Multiplexer
Buffer
Buffer Control Unit
Serial Interface Control Unit
Data Out
Clk Out (Optional)
TX/RX
REG_DATA
Data In
Signal Ground
(Optional)
BC
A (Optional)
Burst Enable
Burst Clock
Recovered DATA
Recovered Clock
Data Send

fig. 3

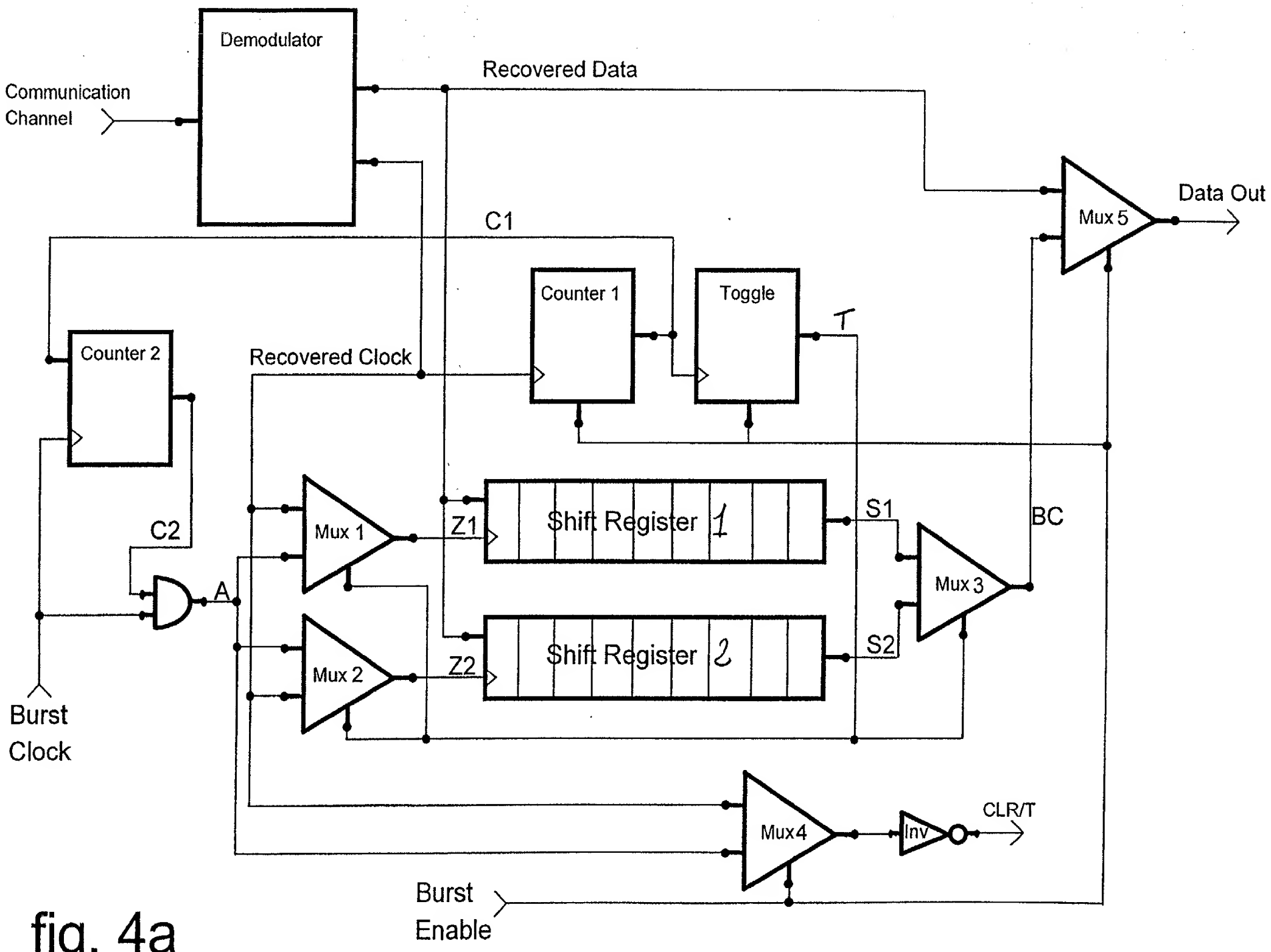

Demodulator
Communication Channel
Recovered Data
C1
Data Out
Mux 5
Counter 1
Toggle
T
Counter 2
Recovered Clock
C2
Mux 1
Z1
Shift Register 1
S1
BC
Mux 3
A
Mux 2
Z2
Shift Register 2
S2
Burst Clock
Mux4
Inv
CLR/T
Burst Enable

fig. 4a

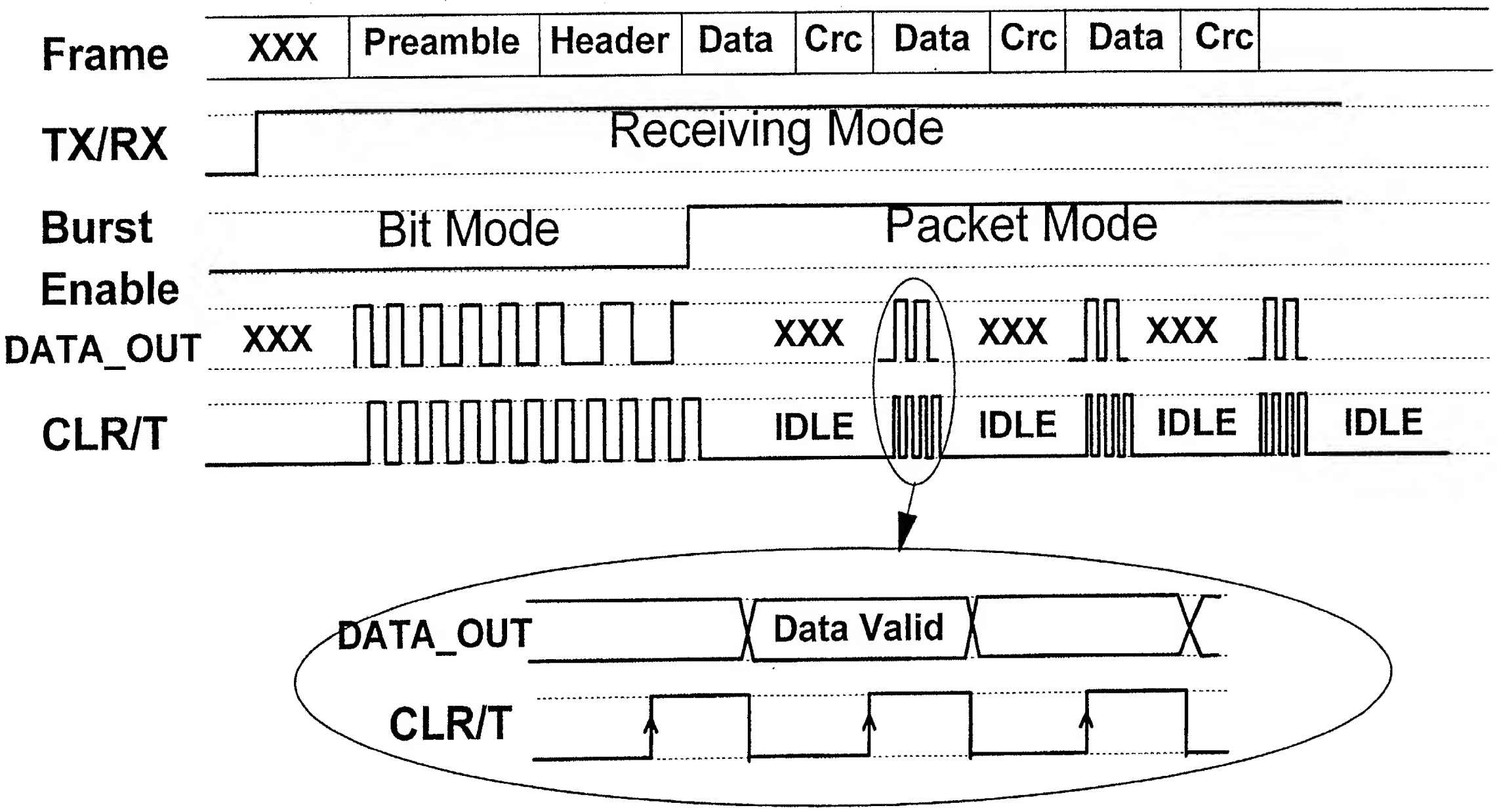
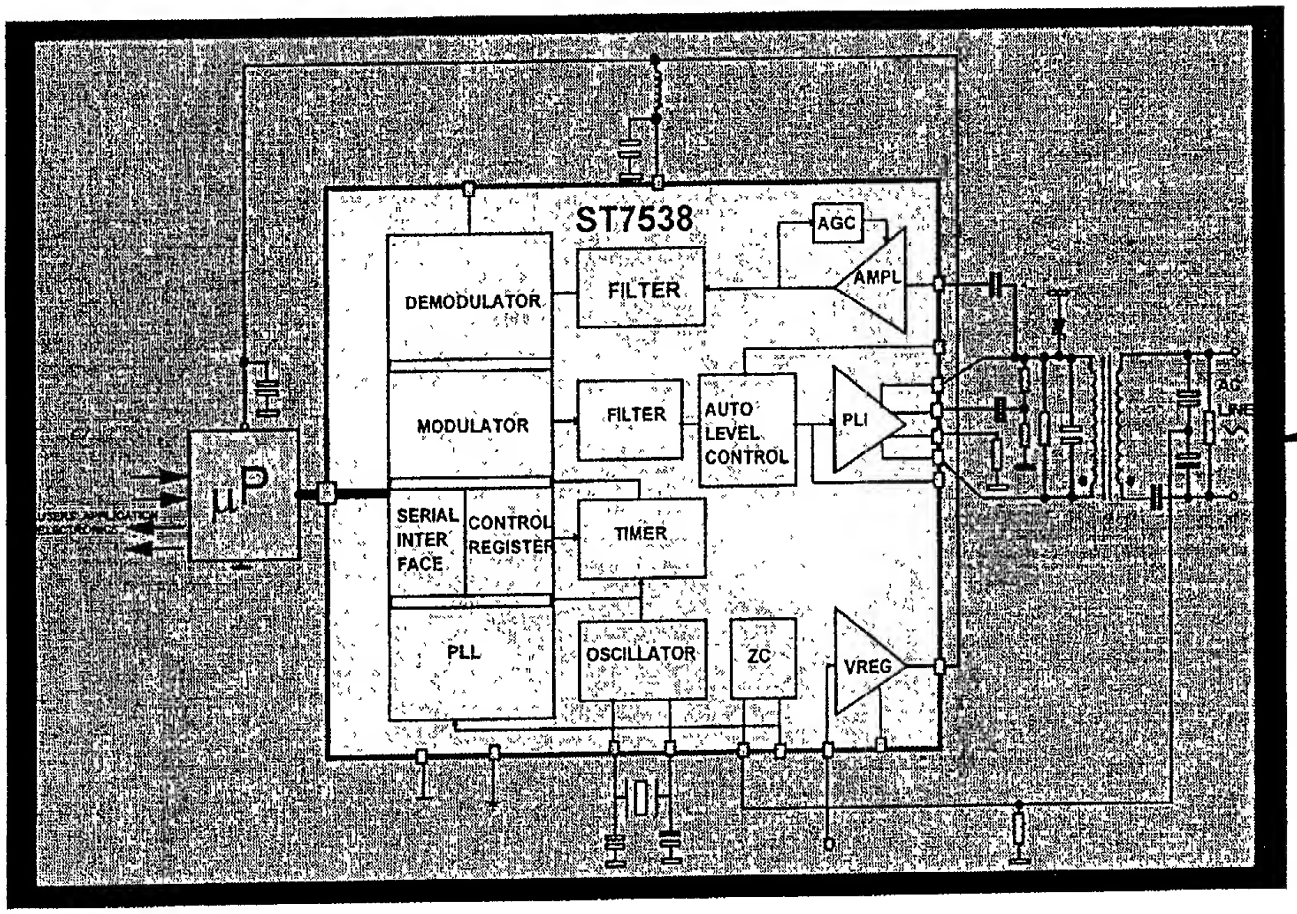

Frame
XXX
Preamble
Header
Data
Crc
Data
Crc
Data
Crc
TX/RX
Receiving Mode
Burst
Bit Mode
Packet Mode
Enable
DATA_OUT
XXX
XXX
XXX
XXX
CLR/T
IDLE
IDLE
IDLE
IDLE
DATA_OUT
Data Valid
CLR/T

fig. 4b

PLM Node



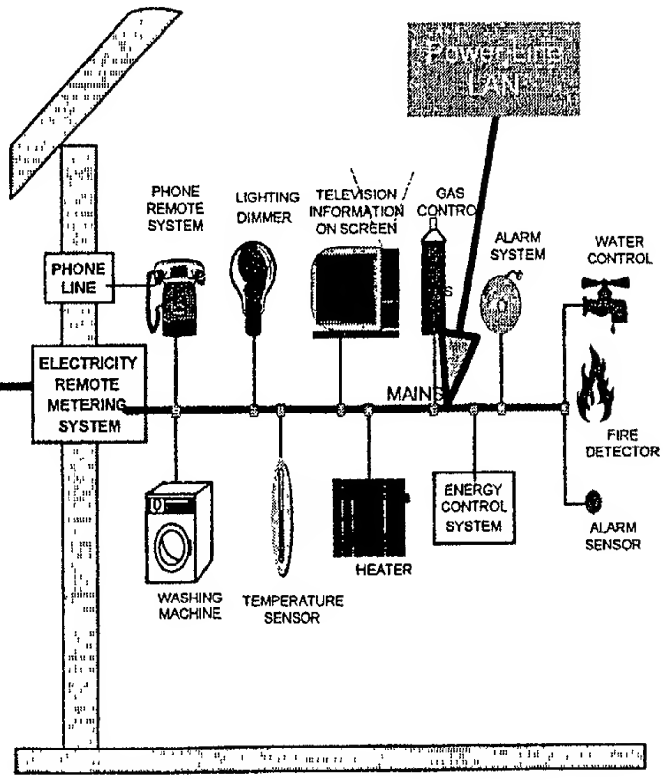


fig. 5a

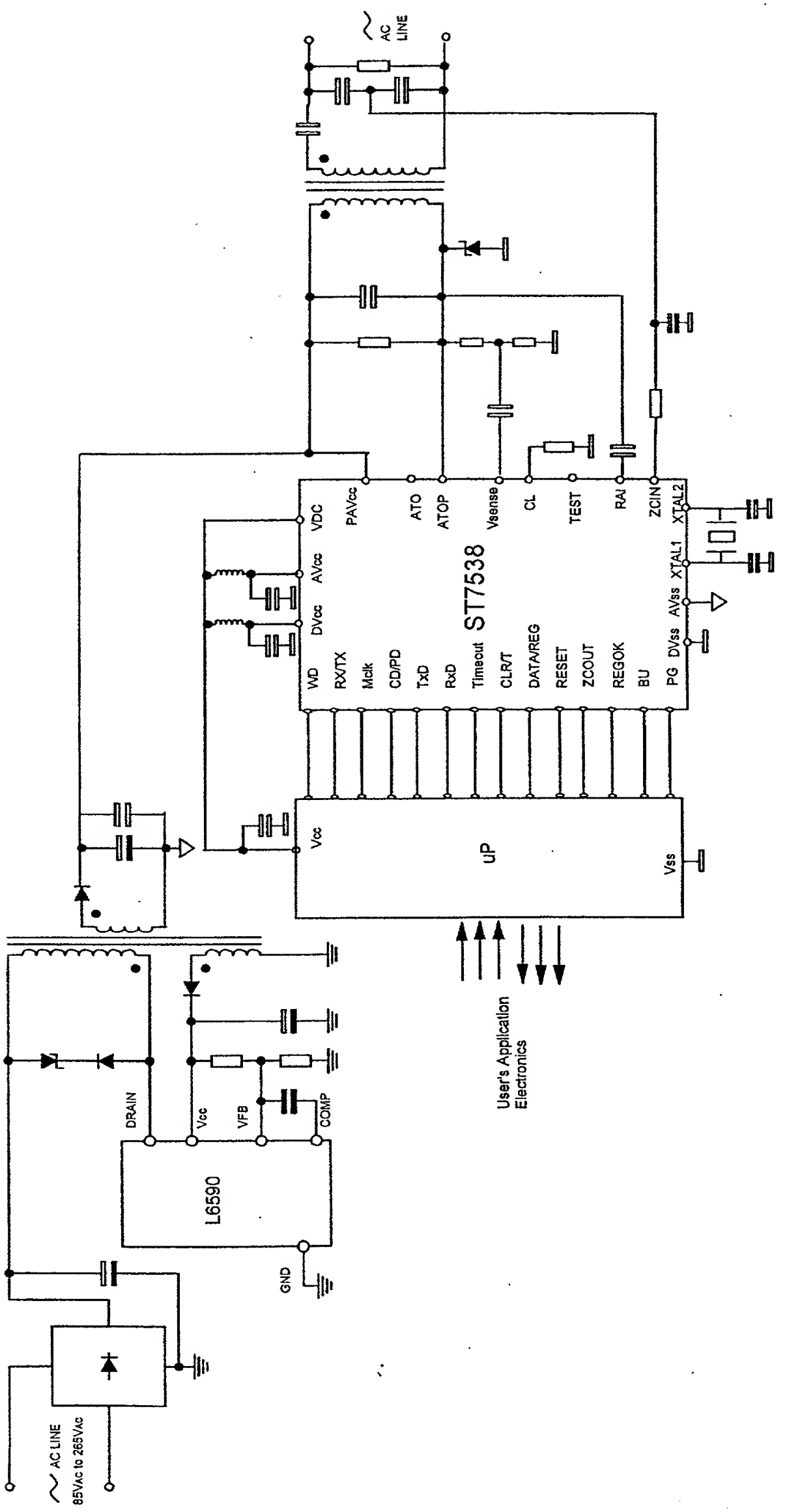

AC LINE
ST7538
VDC
PAVcc
ATO
ATOP
Vsense
CL
TEST
RAI
ZCIN
XTAL2
XTAL1
AVss
DVss
AVcc
DVcc
WD
RX/TX
Mclk
CD/PD
TxD
RxD
Timeout
CLR/T
DATA/REG
RESET
ZCOUT
REGOK
BU
PG
uP
Vcc
Vss
User's Application Electronics
L6590
DRAIN
Vcc
VFB
COMP
GND
AC LINE
85Vac to 265Vac

fig. 5b